This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor memory integrated circuit comprising:

a semiconductor substrate;

a device isolation insulating film buried in grooves formed into said semiconductor substrate;

a cell array having an arrangement of electrically erasable and programmable ~~nonvolatile memory cells made by stacking floating gates and control gates on said~~ semiconductor substrate; and

a peripheral circuit disposed around said cell array on said semiconductor substrate,

at least the bottom layer of said floating gates of said nonvolatile memory cells and at least the bottom layer of gate electrodes of transistors in said peripheral circuit being formed before said device isolation insulating film is buried, then the bottom layer of said floating gates of said nonvolatile memory cells and the bottom layer of gate electrodes of transistors in said peripheral circuit being maintained in self alignment with said device isolation insulating film, N type impurities being doped into the gate electrodes of NMOS transistors and P type impurities being doped into the gate electrodes of PMOS transistors in said peripheral circuit ~~and impurities being doped thereto under different conditions from each other~~.

2. (Currently Amended) The semiconductor memory integrated circuit according to claim 1 wherein two kinds of ~~said~~ transistors, thicknesses of the two kinds of transistors being different from each other, are arranged in the ~~in said~~ peripheral circuit ~~have at least two gate insulating films different in thickness~~.

3. (Original) The semiconductor memory integrated circuit according to claim 1,

wherein different n-type impurities are doped into said floating gates of said nonvolatile memory cells and gate electrodes of NMOS transistors in said peripheral circuit, and a p-type impurity is doped into said gate electrodes of PMOS transistors in said peripheral circuit.

4. (Original) The semiconductor memory integrated circuit according to claim 1, wherein phosphorus is doped into said floating gates of said nonvolatile memory cells.

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5. (Original) The semiconductor memory integrated circuit according to claim 1, wherein phosphorus is doped into said floating gates of said nonvolatile memory cells, and arsenic is doped into said gate electrodes of NMOS transistors in said peripheral circuit.

6. (Currently Amended) The semiconductor memory integrated circuit according to claim 1 wherein said floating gates of said nonvolatile memory cells comprise ~~of~~ a first-layer gate electrode material film in self alignment with said device isolation insulating film and a second-layer gate electrode material film stacked on said first gate electrode material film, said control gates comprise ~~of~~ a third-layer electrode material film, and said gate electrodes in said peripheral circuit have a three-layered structure including said first- to third-layer gate electrode material films.

7-20. (Withdrawn)